HIGHER TECHNICAL INSTITUTE

ELECTRICAL ENGINEERING DEPARTMENT

DIPLOMA PROJECT

SIMULATION OF COMMUNICATION SYSTEMS USING MATLAB AND FPGAs

E:1413

CONSTANTINOU MARIOS

JUNE 2007

HIGHER TECHNICAL INSTITUTE
PROJECT NO
3712

HIGHER TECHNICAL INSTITUDE

ELECTRICAL ENGINEERING DEPARTMENT

DIPLOMA PROJECT

SIMULATION OF COMMUNICATION SYSTEMS USING MATLAB AND FPGAs

E1418

CONSTANTINOU MARIOS

JUNE 2007

HIGHER TECHNICAL INSTITUTE | PROJECT NO 3712

SIMULATION OF COMMUNICATION SYSTEMS USING MATLAB AND FPGAs

By

Constantinou Marios

Project report submitted to the

Department of Electrical Engineering

Nicosia – Cyprus

in partial fulfillment of the requirements for the diploma of

TECHNICIAN ENGINEER

in

ELECTRICAL ENGINEERING

June 2007

HIGHER TECHNICAL INSTITUTE
PROJECT NO
3712

ABSTRACT

Simulation of communications systems using MATLAB and FPGAs

by

Constantinou Marios

The main focus of this report is to demonstrate how MATLAB and FPGAs can be used in simulation and implementation of communications systems. Through several demonstrations the author will try to show some applications of MATLAB and FPGA in communication systems.

ACKNOWELEDGEMENTS

I would like to express my sincere appreciation to Mr D Lambrianides Lecturer at the HTI, for his guidance during the preparation of this report

Dedicated to
my friends and my family

CONTENTS

ABSTRACT I

ACKNOWELEDGEMENTS II

CONTENTS IV

LIST OF FIGURES VII

ABBREVIATIONS IX

1. INTRODUCTION TO MATLAB 1

1.1 AIMS AND OBJECTIVES 1
1.2 WHAT IS MATLAB? 1
1.3 MATLAB ENVIRONMENT 2
1.4 INTRODUCTION TO MATLAB EDITOR 3
1.4.1 Starting the MATLAB editor 3
1.4.2 MATLAB Editor 4
1.5 SIMULINK 5
1.5.1 What Is Simulink? 5
1.5.2 Starting Simulink 5
1.5.3 Creating an empty model 6
1.5.4 Adding objects to the model 6
1.5.5 Connecting blocks 7
1.6 TOOLBOXES 7
1.6.1 COMMUNICATIONS TOOLBOX 8
1.6.2 RF TOOLBOX 8
1.6.3 SIGNAL PROCESSING TOOLBOX 8
1.7 BLOCKSETS 8

2. DIGITAL COMMUNICATION 9

2.1 CONSTELLATION DIAGRAM 9
2.2 EYE DIAGRAM 10
2.3 DIGITAL MODULATION 11
2.3.1 Phase-Shift Keying (PSK) 13
2.3.1.1 Binary phase-shift keying (BPSK) 13
2.3.1.2 Quadrature phase-shift keying (QPSK) 14
2.3.2 Frequency-Shift keying (FSK) 16
2.3.2.1 Minimum frequency-shift keying(MSK) 16
2.3.2.2 Audio frequency-shift keying (AFSK) 17
2.3.3 Amplitude-Shift Keying (ASK) 17
2.3.3.1 On – off keying (OOK) 17
2.3.4 Quadrature Amplitude Modulation (QAM) 18

3. EYE DIAGRAM AND SCATTER PLOT FUNCTIONS USING MATLAB 19

3.1 PLOTTING OF A SIGNAL 19
3.2 CREATE AN EYE DIAGRAM 20
3.3 EYE DIAGRAM OF A REAL SIGNAL 21
3.4 EYE DIAGRAM OF YY 22
3.5 MULTIPLE SYMBOLS IN A TRACE 23
3.6 ADJUST THE OPEN PART OF THE EYE 24

3.7 SCATTER PLOT 25
3.8 IN PHASE VS QUADRATURE COMPONENT 26
3.9 SUMMARY 26

4. MSK MODULATION AND DEMODULATION MODEL USING SIMULINK. 27

4.1 BUILDING THE MODEL 27
4.2 RUNNING SIMULATION 30
4.2.1 Scope 30
4.2.2 Spectrum scope 30
4.2.3 Scatter plot 31
4.2.4 Eye diagram 31
4.2.5 Bit Error Rate 31
4.3 ENHANCING THE MODEL 32
4.3.1 Creation of digital Lowpass filter using FDAtool 32
4.3.2 Addition of a delay block 32
4.3.3 RUNNING SIMULATION OF THE ENHANCING MODEL 34
4.3.3.1 SCOPE 34
4.3.3.2 SPECTRUM SCOPE 34
4.3.3.3 Scatter plot 35
4.3.3.3 Eye diagram 35
4.4 OBSERVATIONS 36
4.5 CONCLUSION 36

5. INTRODUCTION TO FPGAS 37

5.1 AIMS AND OBJECTIVES 37
5.2 WHAT IS AN FPGA ? 37
5.3 FPGA APPLICATION AREAS 37
5.4 COMPARING FPGA AND ASICS 38

6. XILINX ISE 9.1 39

6.1 INTRODUCTION 39
6.1.1 Design entry 39
6.1.2 Synthesis 39
6.1.3 Implementation 39
6.1.4 Verification 39
6.1.5 Device configuration 39
6.2 ISE 9.1 ENVIRONMENT 40
6.2.1 Project Navigator Main Window 40
6.2.2 Using the Sources Window 40
6.2.3 Using the Processes Window 41
6.2.4 Process Status 42
6.3 STARTING NEW PROJECT 43

7. CHOOSING OF FPGA 48

8. SCHEMATIC COMBINATIONAL LOGIC DESIGN 49

8.1 ASSIGN PACKAGE PINS 50
8.2 GENERATE THE PROGRAMMING FILE TO FPGA 52

9. COUNTER DESIGN 57

OBJECTIVE OF THIS DEMONSTRATION IS TO CONSTRUCT 28-BIT BINARY COUNTER. 57
9.1 SCHEMATIC DIAGRAM 57
9.1.1 Counter 57
9.1.2 Fourbit 57

9.1.3 fsh 58
9.1.4 HEX2LED VHDL module 58
10.2 PINOUTS 60
HEX2LED MODULE CONVERTS 4BITS TO 7 SEGMENT OUTPUT 60
10.3 TESTING 60
10. FSK MODULATOR DESIGN 61
10.1 SCHEMATIC DIAGRAMS 61
10.1.1 FSK 61
10.1.2 mux 61
10.1.3 freqdiv 62
10.1.4 cnter 62
10.1.5 Testing 62
10.2 PINOUTS 63
11.OOK MODULATOR USING MATLAB SYSTEM GENERATOR 64
11.1 INTRODUCTION TO SYSTEM GENERATOR 64
11.1.1 System Level Modeling with System Generator 64
11.1.2 The System Generator Design Flow 65
11.2 OOK MODULATOR 65
11.2.1 Schematic 65
11.2.2 Simulation 66
11.2.2 Generate HDL Netlist 66
11.3 PINOUTS 67
11.4 TESTING 67
12. COMPARING MATLAB SYSTEM GENERATOR AND XILINX ISE 68
12.1 SIMILARITIES 68
12.2 ADVANTAGES AND DISADVANTAGES OF MATLAB SYSTEM GENERATOR 68
12.3 ADVANTAGES AND DISADVANTAGES OF ISE 9.1 68
13. CONCLUSIONS 69
REFERENCES 71
BIBLIOGRAPHY 72
APPENDICES 73