

DIGITAL FREQUENCY MULTIPLIER

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ABSTRACT in part satisfaction of the award of

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ABSTRACT

This project deals with the designing , construction and testing of a digital frequency multiplier for academic using purpose.

The requirements of this project are :

1. To design the frequency multiplier to be based on a phase lock loop (PLL).
2. To use an X-OR gate for the phase detector of the PLL and ,
3. To examine the operation and characteristics of the PLL.

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